REMARKS

Claims 1-26 were pending in the application prior to the present response. Claims 1-26 have been rejected. Claims 2, 14, 18 and 21 are hereby canceled; claims 1, 13, 17, 20, 24 and 26 are hereby amended; and claim 27 is newly added. Applicants respectfully request the allowance of each of pending claims 1, 3-13, 15-17, 19, 20, and 22-27.

With respect to the specific paragraphs of the Office action, Applicants offer the following specific remarks in support of the patentability of the claims of the present invention.

I. Rejection of Claims 1-26 under 35 U.S.C. § 112, second paragraph

In the Office action, specifically in paragraph 3, claims 1-26 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. In particular, the Examiner cited specific language in claims 1, 13, 17, 24 and 26 as being indefinite. Responsive to the Examiner's comments, each of the aforementioned claims have been amended and now comply with the requirements of 35 U.S.C. § 112, second paragraph. Since independent claims 1, 13, 17 and 24 now comply with the requirements of 35 U.S.C. § 112, second paragraph, and since dependent claim 26 has also been amended and complies with the requirements of 35 U.S.C. § 112, second paragraph, the rejection of claims 1-19 and 24-26, should be under 35 U.S.C. § 112, second paragraph, should be withdrawn.

Independent claim 20, and claims 21-23, which depend from claim 20, were not specifically rejected in this paragraph. Applicants respectfully submit that claims 20-23 each also comply with the requirements of 35 U.S.C. § 112, second paragraph, since the Examiner did not point to any particular grounds of rejection for these claims.

As such, each of claims 1-26 are in compliance with 35 U.S.C. § 112, second paragraph, and the rejection of claims 1-26, under 35 U.S.C. § 112, second paragraph, should be withdrawn.

II. Rejection of Claims 1-6, 10-15, 17-22 and 24-26 under 35 U.S.C. § 103(a)

In the Office action, specifically in paragraph 4, claims 1-6, 10-15, 17-22 and 24-26 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Yu, U.S. Patent No. 6,399,450, in view of Shiozawa et al., U.S. Patent No. 5,970,352, hereinafter "Shiozawa". These claim rejections are overcome based on the claim amendments and the remarks set forth below.

Neither of the references of Yu or Shiozawa teach the use of laser annealing to drive impurities from a film into another film, or from a film into the substrate.

Furthermore, neither of the references of Yu or Shiozawa teach a step of converting a film from an amorphous structure to a crystalline or polysilicon structure while, during this conversion step, also driving impurities from the amorphous film into another region such as a source/drain region of a substrate.

Therefore neither of the references teach the use of laser annealing to convert an amorphous silicon layer to a crystalline or polycrystalline laser while also driving impurities from the layer, into another layer or surface.

Yu does not teach or suggest the diffusion of impurities species during the step used to convert the amorphous film. Yu further does not disclose or suggest the use of laser annealing to urge the diffusion of impurity species from one layer to another.

The cited reference of Shiozawa does not disclose or suggest laser annealing at all. Shiozawa forms an amorphous silicon film then converts the film to a polysilicon section and a single crystalline section. "[A]nnealing process is carried out . . . . As a result of this annealing process, the amorphous silicon film 141 is epitaxially regrown in areas where the crystalline structure of semiconductor substrate 115 provides a seed for crystallization of the overlying amorphous silicon. In areas where semiconductor substrate 115 does not provide a seed for crystallization, the amorphous silicon is converted to a polysilicon film 143.", col. 5, lines 22-30. After the conversion step, Shiozawa forms a further film over the converted film and then uses multiple anneal steps at elevated temperatures to urge the diffusion of dopant impurity species. "[I]mpurity doped film 147 is formed on polysilicon film 143 and epitaxial film 145" col. 5, lines 38-39; and " an annealing process is carried out at . . . . about 950°C . . . .

to diffuse impurities from impurity doped film 147 to polysilicon film 143 and epitaxial film 145" col. 5, lines 58-62. Shiozawa does not disclose the use of laser annealing, much less the use of laser annealing to urge the diffusion of dopant impurity species. Shiozawa further does not disclose or suggest the diffusion of dopant impurity species <u>during</u> the step used to convert the amorphous silicon layer to a polysilicon/single crystalline layer.

This application contains independent claims 1, 3, 17, 20 and 24. Claims 1, 13, 17 and 20 have been amended. Each of independent claims 1, 13, 17, 20 and 24 include the feature that, <u>*while the amorphous silicon layer is being converted to a crystalline structure, dopant impurities are urged from the layer into the substrate*</u>. Claims 1, 13, 17, 20 and 24 are therefore distinguished from the references of Yu and Shiozawa. Each of independent claims 1, 17, 20 and 24 also include the feature that this conversion process is carried out by selective laser annealing.

In particular, claims 1, 13 and 17 each recite the feature that:

"converting said amorphous silicon . . . . to a crystalline silicon . . . . , said converting urging at least some of said dopant impurities to diffuse into said source/drain region."

Amended claim 20 recites the feature of:

"selectively laser annealing said discrete amorphous silicon layer, thereby converting said discrete amorphous silicon layer to a discrete single crystalline silicon layer and driving at least some of said dopant impurities into said exposed surface."

Similarly, claim 24 recites the feature of:

"irradiating with a laser beam, then allowing cooling, thereby converting said discrete amorphous silicon film to a crystalline silicon film and urging the diffusion of at least some of said dopant impurities into said source/drain regions."

Claims 24 and amended claims 1, 13, 17 and 20 each therefore recite features neither disclosed nor suggested by the references of Yu or Shiozawa, taken alone or in combination.

Furthermore, each of amended claims 1, 13 and 20 as well as claim 24, further include the distinguishing feature that <u>*the step of converting and urging dopant impurity diffusion is a*</u>

selective laser annealing step. For example, claim 1 recites "converting said amorphous silicon layer to a crystalline silicon layer using selective laser annealing." Claims 1, 13, 20 and 24 are therefore further distinguished from the references.

As above, neither of the references of Yu or Shiozawa disclose the use of laser annealing to urge the diffusion of impurities species, taken alone or in combination. Furthermore, neither of the references of Yu or Shiozawa disclose or suggest the diffusion of impurity species during the step used to convert an amorphous material to a crystalline material.

Therefore, each of amended claims 1, 13, 17 and 20, as well as claim 24, are distinguished from the references of Yu and Shiozawa, taken alone or in combination and therefore the rejection of these claims under Yu in view of Shiozawa, should be withdrawn. Claims 3-6, 10-12, 14, 15, 18, 19, 21, 22, 25 and 26 each depend from one of the aforementioned independent claims and are therefore also distinguished from the cited references of Yu and Shiozawa, taken alone or in combination. Claims 2, 14, 18 and 21 have been canceled.

Therefore the rejection of claims 1, 3-6, 10-13, 15, 17, 19, 22 and 24-26 under 35 U.S.C § 103(a) as being unpatentable over Yu in view of Shiozawa, should be withdrawn.

III. Newly Added Claim 27

Neither of the references of Yu or Shiozawa disclose or suggest a metal gate. Yu teaches a polysilicon gate at column 5, lines 32-33. Shiozawa teaches a polysilicon/silicide/cap portion gate in column 4,lines 5-7. Neither reference suggests a metal gate. In fact, the process sequence of each of the references precludes utilization of a metal gate because of the subsequent high temperatures used for a annealing and activating dopants (950°C anneal in Shiozawa and 1000-1100°C RTA activation process used in Yu), which exceeds the melting temperature of conventionally used metals.

Newly added claim 27 recites the step of forming a metal gate and also the feature that the converting step that uses selective laser annealing, does not melt the metal gate. New claim 27 also includes the feature that a selective laser anneal is used to convert amorphous

silicon to crystalline silicon while urging the out-diffusion of dopant impurities from the silicon, further distinguishing from the references of Yu and Shiozawa. Claim 27 is distinguished from Yu and Shiozawa and therefore in allowable form.

IV. Rejection of Claims 7-9, 16 and 23 under 35 U.S.C. § 103(a)

In the Office action, particularly in paragraph 8, claims 7-9, 16 and 23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Yu and Shiozawa as applied to claims 1-3, 5-6, 9, 11-22 and 24-26 above, and further in view of Kohno, et al., hereinafter "Kohno". These claim rejections are overcome based on claim amendments and the reason set forth below.

With respect to claim 7-9, 16 and 23, the Examiner apparently relies upon Kohno which discloses an XeCl excimer laser that emits light at 308nm. Kohno is not directed to an FET having source/drain regions and does not make up for the deficiencies of Yu and Shiozawa as stated above. Claim 7-9 each depend, directly or indirectly, from amended claim 1, claim 16 depends from amended claim 13 and claim 23 depends from amended claim 20, the independent claims each distinguished from the references of Yu and Shiozawa for reasons set forth above. Claims 7-9, 16 and 23 therefore include features neither disclosed nor suggested in the cited references, taken alone or in combination.

Claim 9 is further distinguished because it recites the feature of a metal transistor gate. In the paragraph regarding claim 9, the Examiner states that Shiozawa teaches providing the transistor comprising a metal gate and directs the reader to column 4, lines 50-65. Applicants respectfully point out that Shiozawa does not disclose a metal gate in this or any other portion of the specification. Shiozawa discloses a polysilicon film and a silicide film in the identified excerpt. Furthermore, if the gate structure of Shiozawa did include virtually any commercially usable metal, Shiozawa's subsequent oxidation step at 1050°C, would melt the metal gate. Shiozawa therefore teaches away from the use of a metal gate. Claim 9 therefore recites a further distinguishing feature neither disclosed nor suggested in Shiozawa.

The rejections of claim 7-9, 16 and 23 under 35 U.S.C § 103(a) as being unpatentable over Yu and Shiozawa in view of Kohno, should be withdrawn.

CONCLUSION

For the foregoing reasons, each of claims 1, 3-13, 15-17, 19, 20 and 22-27 are in allowable form and the application is therefore in condition for allowance, which action is respectfully and expeditiously requested.

Attached herewith is a marked - a version of the changes made to the claims by the current amendments. The attached page is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

Respectfully submitted,

CHRISTIE, PARKER & HALE, LLP

By ______________________

Mark J. Marcelli
Reg. No. 36,593
626/795-9900

MJM/mmf

VERSION WITH MARKINGS TO SHOW CHANGES MADE

Please amend claims 1, 13, 17, 20, 24 and 26 as follows:

1. (Amended) A method for forming a raised source/drain contact structure for a semiconductor transistor, comprising the steps of:

providing a transistor gate on a substrate surface, and a source/drain region defined as a surface region extending laterally from said transistor gate to an isolation structure formed one of on said substrate and in said substrate;

forming [~~an~~] a doped amorphous silicon layer over and contacting said source/drain region and over said isolation structure, said doped amorphous silicon layer including dopant impurities therein;

converting said amorphous silicon layer to a crystalline silicon layer using selective laser annealing, said converting urging at least some of said dopant impurities to diffuse into said source/drain region; and

patterning said crystalline silicon layer to form a raised source/drain contact structure covering said source/drain region and extending over at least part of said isolation structure.

13. (Amended) A method for forming a raised source/drain contact structure for a semiconductor transistor, comprising the steps of:

providing a transistor gate on a substrate surface and a source/drain region, defined as a surface region extending laterally from said transistor gate to an isolation structure formed one of on said substrate and in said substrate;

forming [~~an~~] a doped amorphous silicon layer over and contacting said source/drain region and said isolation structure, said doped amorphous silicon layer including dopant impurities therein;

patterning said amorphous silicon layer to form a raised source/drain contact structure covering said source/drain region and extending over at least part of said isolation structure; and

converting said amorphous silicon raised source/drain contact structure to a crystalline silicon raised source/drain contact structure, said converting urging at least some of said dopant impurities to diffuse into said source /drain region.

17. (Amended) A method for forming a raised source/drain contact structure for a semiconductor transistor, comprising the steps of:

providing a transistor gate on a substrate surface, and opposed source/drain regions, each source/drain region defined as the surface region extending laterally from said gate to a corresponding isolation structure formed one of on said substrate and in said substrate;

forming [~~an~~] a doped amorphous silicon layer over and contacting each said source/drain region and over each said corresponding isolation structure, said doped amorphous silicon layer including dopant impurities therein;

converting said amorphous silicon layer to a crystalline silicon layer using selective laser annealing, said converting urging at least some of said dopant impurities to diffuse into said source/drain regions; and

patterning said crystalline silicon layer to form a duality of raised source/drain contact structures, each covering said corresponding source/drain region and extending over at least part of said [~~associated~~] corresponding isolation structure.

20. (Amended) A method for forming a semiconductor structure, comprising the steps of:

providing an exposed surface of a semiconductor substrate, said exposed surface bounded laterally by at least one isolation structure;

forming a discrete amorphous silicon layer contacting said exposed surface and extending laterally over at least portions of at least one of said at least one isolation structure, said discrete amorphous silicon layer including dopant impurities therein; and

selectively laser annealing said discrete amorphous silicon layer, thereby converting said discrete amorphous silicon layer to a discrete single crystalline silicon layer and driving at least some of said dopant impurities into said exposed surface.

24. (Amended) A method for forming a transistor comprising:

providing a semiconductor substrate having a surface;

providing a transistor region between isolation structures formed in said substrate;

forming a gate stack, including a gate electrode formed over a gate dielectric, in a central portion of said transistor region, said gate stack covered with an insulating material, the lateral portions of said transistor region not covered by said gate stack being designated source/drain regions;

forming a discrete amorphous silicon film over said transistor region, said discrete amorphous silicon film including dopant impurities therein;

irradiating with a laser beam, then allowing cooling, thereby converting said discrete amorphous silicon film to a crystalline silicon film and urging the diffusion of at least some of said dopant impurities into said source/drain regions; and

forming an opposed duality of discrete raised source/drain contact structures from said crystalline silicon film, by removing portions of said crystalline silicon film, each raised source/drain contact structure formed over a corresponding source/drain region.

26. (Amended) The method as in claim 24, further comprising forming a dielectric structure over said surface prior to the step of forming said discrete amorphous silicon film, portions of said dielectric structure encroaching said transistor region and in which said step of forming a discrete amorphous silicon film includes forming said discrete amorphous silicon film over at least portions of said dielectric [~~film~~] structure.

DLF PAS476334.1-*-12/12/02 2:10 PM